CLAIMS

WHAT IS CLAIMED IS:

1. A method comprising:

determining whether an instruction at which an address watch breakpoint occurs is within a hardware synchronization mechanism range in a program; and

if the determining is true, setting a special breakpoint following the hardware synchronization mechanism range.

- The method of claim 1, further comprising:
 if the determining is true, temporarily disabling the address watch breakpoint.
- 3. The method of claim 1, further comprising: detecting whether a processor storage reservation indicator has been cleared during processing of the address watch breakpoint.
- The method of claim 1, further comprising:
 if the determining is true, saving a machine state.
- 5. The method of claim 4, further comprising:

 presenting the machine state after the special breakpoint is encountered.

6. An apparatus comprising:

means for determining whether an instruction at which an address watch breakpoint occurs is within a hardware synchronization mechanism range in a program;

means for setting a special breakpoint following the hardware synchronization mechanism range if the means for determining is true; and

means for temporarily disabling the address watch breakpoint if the means for determining is true.

7. The apparatus of claim 6, further comprising:

means for detecting a clearing of a processor storage reservation indicator after the instruction at which the address watch breakpoint occurs is encountered.

8. The apparatus of claim 6, further comprising:

means for saving a machine state if the means for determining is true.

9. The apparatus of claim 8, further comprising:

means for determining whether a processor storage reservation indicator is set after encountering an end of the hardware synchronization mechanism range.

10. The apparatus of claim 9, further comprising:

means for presenting the machine state after the special breakpoint is encountered if the processor storage reservation indicator is set.

11. A signal-bearing medium encoded with instructions, wherein the instructions when executed comprise:

determining whether an instruction at which an address watch breakpoint occurs is within a hardware synchronization mechanism range in a program;

setting a special breakpoint following the hardware synchronization mechanism range if the determining is true;

temporarily disabling the address watch breakpoint if the determining is true; and saving a machine state if the determining is true.

12. The signal-bearing medium of claim 11, further comprising:

detecting a clearing of a processor storage reservation indicator after the instruction at which the address watch breakpoint occurs is encountered.

- 13. The signal-bearing medium of claim 11, further comprising:

 determining whether a processor storage reservation indicator is set after encountering an end of the hardware synchronization mechanism range.
- 14. The signal-bearing medium of claim 11, wherein the special breakpoint comprises pointers to the machine state and the instruction at which the address watch breakpoint occurred.
- 15. The signal-bearing medium of claim 13, further comprising:

 presenting the machine state after the special breakpoint is encountered if the processor storage reservation indicator is set.
- 16. A computer system comprising:

a processor; and

a main memory encoded with instructions, wherein the instructions when executed on the processor comprise:

determining whether an instruction at which an address watch breakpoint occurs is within a hardware synchronization mechanism range in a program,

setting a special breakpoint following the hardware synchronization mechanism range if the determining is true,

temporarily disabling the address watch breakpoint if the determining is true,

saving a machine state if the determining is true, and determining whether a processor storage reservation indicator is set after encountering an end of the hardware synchronization mechanism range.

17. The computer system of claim 16, wherein the instructions further comprise: detecting a clearing of the processor storage reservation indicator after the instruction at which the address watch breakpoint occurs is encountered.

- 18. The computer system of claim 16, wherein the instructions further comprise:

 presenting the machine state if the processor storage reservation indicator is set after encountering an end of the hardware synchronization mechanism range.
- 19. The computer system of claim 16, wherein the instructions further comprise: presenting the machine state after the special breakpoint is encountered if the processor storage reservation indicator is set.
- 20. The computer system of claim 16, wherein the special breakpoint comprises pointers to the machine state and the instruction at which the address watch breakpoint occurred.